What is claimed is:

1. An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, each one of the outer pair being formed adjacent to and on opposing sides of the inner plug, each one of the outer pair having upper portions, wherein the upper portions cover areas of the surface structures; and

an inner electrical contact coupling to the inner plug and separated from the upper portions by a pair of opposing spacers.

2. The device of claim 1, wherein the device further includes a pair of outer contact regions, wherein each of the outer contacts individually couples to one of the outer pair of plugs.

3. The device of claim 2, wherein the pair of outer plugs include storage node plugs, and wherein the outer contact regions include storage nodes.

4. The device of claim 1, wherein the number of semiconductor surface structures includes isolated wordlines.

5. The device of claim 1, wherein the number of semiconductor surface structures includes isolated flash memory cells.

6. The device of claim 1, wherein the inner plug is formed beneath a top surface of the number of semiconductor surface structures.

7. The device of claim 1, wherein the number of plugs include polysilicon plugs.

8. The device of claim 1, wherein the inner plug includes a bitline plug, and wherein the inner electrical contact includes a bitline contact.

9. The device of claim 1, wherein the device includes a dynamic random access memory (DRAM).

10. The device of claim 1, wherein the device includes a synchronous random access memory (SRAM).

11. A memory device, comprising:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent pair of insulated wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the adjacent pair of insulated wordlines, wherein the spacer isolate the buried bitline from the pair of storage node plugs.

12. The memory device of claim 11, wherein the bitline plug includes polysilicon.

13. The memory device of claim 11, wherein the pair of storage node plugs includes polysilicon.

14. The memory device of claim 11, wherein the memory device further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

15. The memory device of claim 11, wherein the memory device includes a dynamic random access memory (DRAM).

16. The memory device of claim 11, wherein the memory device includes a synchronous random access memory (SRAM).

17. A data handling system, comprising:

a central processing unit;

a memory device, wherein the memory device comprises:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent wordlines from the bitline plug, wherein the pair of storage node plugs each have a top surface above the top surfaces of the insulated wordlines and are formed over portions of the adjacent wordlines;

a buried bitline coupled to the bitline plug; and

a pair of opposing spacers located above the pair of adjacent wordlines and isolating the buried bitline from the pair of storage node plugs; and

a system bus for communicatively coupling the central processing unit and the memory device.

18. The data handling system of claim 17, wherein the bitline plug includes polysilicon.

19. The data handling system of claim 17, wherein the pair of storage node plugs includes polysilicon.

20. The data handling system of claim 17, wherein the memory device further includes a pair of storage node contacts, wherein each of the storage node contact individually couples to one of storage node plugs.

21. The data handling system of claim 17, wherein the memory device includes a dynamic random access memory (DRAM).

22. The data handling system of claim 17, wherein the memory device includes a synchronous random access memory (SRAM).